PAPER ID-421487

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM IV) THEORY EXAMINATION 2021-22
DIGITAL ELECTRONICS

Time: 3 Hours ***Total Marks: 100***

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 *10 = 20

Q no.	Question	CO
a.	Identify the value of x in the expression $(56.1A)_{16} = (x)_8$.	1
b.	Perform the subtraction $(101101\text{-}100110)_2$ using 2's complement method.	1
c.	Compare serial adder and parallel adder.	2
d.	What is difference between combinational and sequential circuits.	2
e.	The content of 4 bit register is initially 1101. The register is sifted six time to right with the serial input being 101101. What is the content of the register after sixth shift?	3
f.	If in an edge triggered JK flip flop, J=1, K=1 and Q=1, when the clock pulse goes HIGH, what would be the next sate of Q.	3
g.	Define critical race and non-critical race conditions.	4
h.	Differentiate synchronous and asynchronous sequential circuits.	4
i.	Write the advantage and disadvantages of TTL and CMOS logic family	5
j.	Explain fan-in and fan-out in logic families.	5

SECTION B

2. Attempt any *three* of the following: 10*3 = 30

Q no.	Question	CO
a.	Simplify the following Boolean function using K-map and also draw the simplified logic circuit using basic logic gates. $f(A,B,C,D) = \sum_m (0,1,5,6,12,13,14) + d(2,4)$	1
b.	Implement the function $Y(A,B,C,D) = \sum_m (0,1,2,5,8,13,14)$ using 8:1 multiplexer. Consider A, B, C as the select lines.	2
c.	Differentiate between synchronous and asynchronous counters. Design a 2 bit synchronous UP counter.	3
d.	An asynchronous sequential circuit with two excitation function with two feedback loop is given as: $Y_1 = xy_1 + \bar{x}y_2$; $Y_2 = x\bar{y}_1 + \bar{x}y_2$ (i) Draw the logic diagram of the circuit. (ii) Derive the transition table & obtain the flow table	4
e.	Differentiate RAM and ROM. Explain various types of ROM.	5

SECTION C

3. Attempt any *one* part of the following: 10*1 = 10

Q no.	Question	CO
a.	Explain Error detecting and Error correcting codes. A seven-bit Hamming code coming out of a transmission line is 1000010. What was the original code transmitted? Consider the even parity check.	1
b.	Express the design of Ex-OR gate with the help of (i) NAND gates only and (ii) NOR gates only	1

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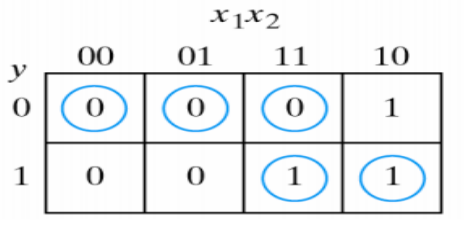
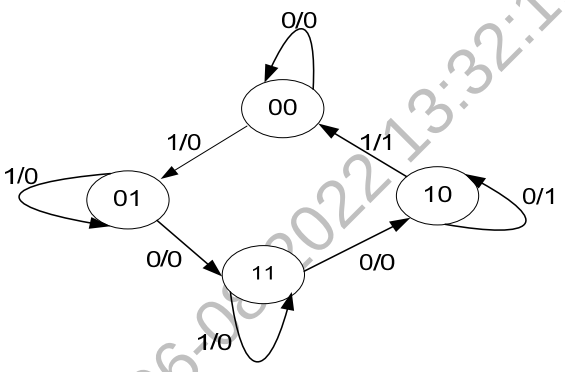
4. Attempt any *one* part of the following: 10*1 = 10

Q no.	Question	CO
a.	Explain the design of a Full adder, with its truth table and Boolean expression.	2
b.	Design a Binary Code to Gray code Converter, Also show its truth table, Boolean expression and logic diagram.	2

5. Attempt any *one* part of the following: 10*1 = 10

Q no.	Question	CO
a.	Discuss the Race around condition of JK flip flop. How JK flip-flop can be used as T flip-flop, Explain the design procedure.	3
b.	Analyze RS flip –flop using NAND-NAND logic and obtain its characteristic equation and excitation table. Explain how will you convert it in D Flip-flop.	3

6. Attempt any *one* part of the following: 10*1 = 10

Q no.	Question	CO
a.	Implement the circuit defined by the following transition table with a NOR SR Latch. Also show the implementation with NAND SR latch. 	4
b.	Write the design procedure for clocked sequential circuits and implement the following state diagram. 	4

7. Attempt any *one* part of the following: 10*1 = 10

Q no.	Question	CO
a.	Explain PLA and PAL. Implement the given Boolean function with a PLA. $Y_1(A,B,C) = \sum_m (4,5,7)$; $Y_2(A,B,C) = \sum_m (3,5,7)$	5
b.	Construct the following logic gates from NMOS and PMOS logic Families (i) NAND (ii) NOR	5